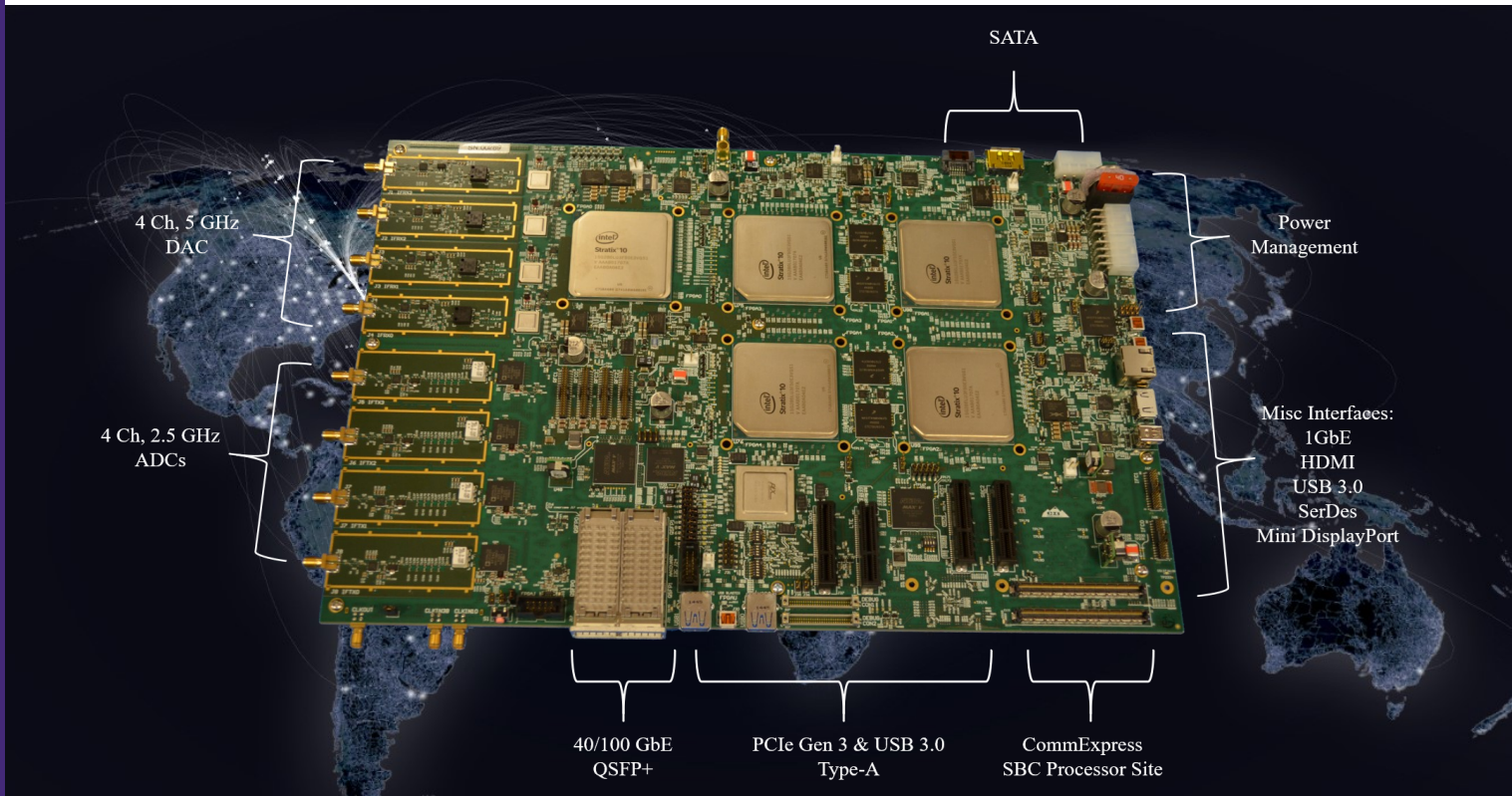


Peregrine I - DREX/SDR

High Performance Digital Receiver/Exciter/Software Defined Radio



PRODUCT DESCRIPTION

CEI's Peregrine I Digital Receiver/Exciter (DREX) provides 7.5 TFLOPS in a 10"x16" package. Peregrine I is equipped with an Intel i7 processor site, five Intel Arria 10 FPGAs, multiple banks of DDR3, four 2.5 GSPS ADC channels, four 5 GHz DAC channels, multiple PCIe Gen 3 interfaces and two 40/100 GbE QSFP+ interfaces. Other features include HDMI, USB3.0, and Gigabit Ethernet. Equipped with massive amounts of processing power and DSP capability, Peregrine I is unlike any other digital receiver/exciter platform on the market!



FPGA Design
Solutions Network
Platinum

SPECIFICATIONS

Arria 10 FPGAs

- 10AX115SF45 (L-tile)
- 72 XCVR
- 1.2 M logic elements
- 3,036 18x19 multipliers

I/O FPGA (FPGA0)

- PCIe Gen3x4
- 10 GB/s FPGA-to-FPGA SERDES crossbar
- 4 GB DDR3 with ECC
- 2x QSFP 40 GbE
- JESD204B interface to ADCs
- LVDS interface to DACs

Processing FPGAs (FPGA1-4)

- PCIe Gen3x4
- 10 GB/s FPGA-to-FPGA SERDES crossbar
- 15 GB/s FPGA SERDES ring (1 < 2 < 3 < 4 < 1)
- 4 GB DDR3 with ECC
- 30x GPIO crossbar **DAC (AD9119)**
- 11-bit 5.7 GS/sec
- LVDSx22
- **ADC (AD9625)**
- 12-bit 2.5 GS/sec
- JESD204B - 8 lanes @ 6.25 Gbps

SBC (COM EXPRESS INTEL i7-4700EQ)

- 1x PCIe Gen3x4 to FPGAs
- 3x PCIe Gen3x2 slots
- GbE
- 2x USB 3.0
- 1x SATA
- 1x HDMI
- 1x mini DisplayPort

Model Number	Configuration
P1-A10	5x Arria 10 FPGAs
P2-S10	5x Stratix 10 FPGAs

BLOCK DIAGRAM/ACTUAL PHOTO WITH SBC

