3DR COMPUTING

Thunder II

8 Channel, 16-bit, 11.5 GSPS Digital-to-Analog Converter

Model Number: 3DR-A10-DAC-11.5 GSPS

COLORADO ENGINEERING, Inc.

3D COMPUTING OVERVIEW

3DR Computing technology brings together high performance computing, ease of programmability, low-cost, and commercial I/O flexibility in a modular, open systems and standards architecture to realize uniquely scalable and widely configurable, high speed embedded processing solutions for the development of radar, EW, SIGINT, and communication systems. 3DR Computing possesses the unique ability to morph in size, shape, and processing capacity. This flexibility provides a low cost, standard solution capable of rapidly conforming to the vastly different power, space, and environmental requirements found aboard any surface, sub-surface, or airborne system or platform.

PRODUCT DESCRIPTION

The 3DR-A10-DAC-11.5 GSPS, known as Thunder II, is an eight channel, 16 bit, 11.5 GSPS Digital-to-Analog Converter board used to convert digital signals into analog waveforms. The on-board Intel Arria 10 FPGA (10AX115U2F45I2SG) can be used to digitally generate waveforms or playback pre-stored samples. As with all 3DR Computing modules, Thunder II supports three-dimensional connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements. Thunder II also offers additional external interface via SMA for tailored clocking and control signal flexibility. The 3DR Computing standard microcontroller architecture is interfaced through the I2C bus to provide FPGA temperature, voltage, and current monitoring for automatic shut-down during critical over heat and/or voltage conditions.

FEATURES

FPGA

- Intel Arria 10
- 10AX115U2F45I2SG
- JTAG Programmable

I/O Support available via

- Y-Connector (2x)
- Z-Connector (1x)
- JTAG
- UART
- RGMII (RJ45)

Tailored Clocking and Control Signal Flexibility

- Clock Input (SMA)
- SPI Programmable HMC7044 to Generate High Fidelity JESD204B Clock Network

Digital –to-Analog Conversion

- AD9172
- 8 Channel
- 16-bit

Standard 3D Computing

Microcontroller Interface

- K61 µ Controller
- Controls Power-on and Power-down Sequencing
- Monitors Voltages and Reports Faults
- Monitors Current, E-fuse Shut-down
- Monitors Board Temperature
- On-board EEPROM for Data Storage and Logging (Write Protect Available)
- Internal FRAM Memory

CLPD

MaxV Reset CPLD

- Reset Control/Interrupt Monitoring
- 1.8/3.3V Standard I/O
- MCU SPI Fanout
- JTAG Programmable
- Internal NOR Flash Memory

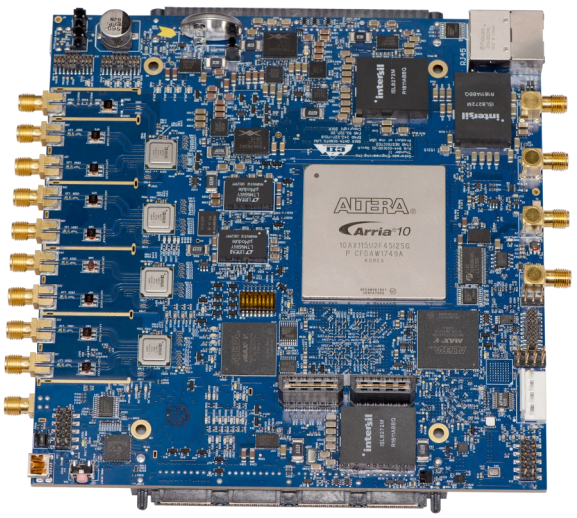
MaxV JTAG CPLD

- JTAG Chain Establishment and Control
- FPGA Reset CPLD Programming via JTAG

intel FPGA Design Solutions Network Platinum

APPLICATIONS

- General Purpose/ Digital Signal Processing
- Radar Exciters and Digital Waveform Generation (DWG)
- Electronic Warfare/Attack Systems
- SIGINT (ELINT, COMINT, Etc.) Systems



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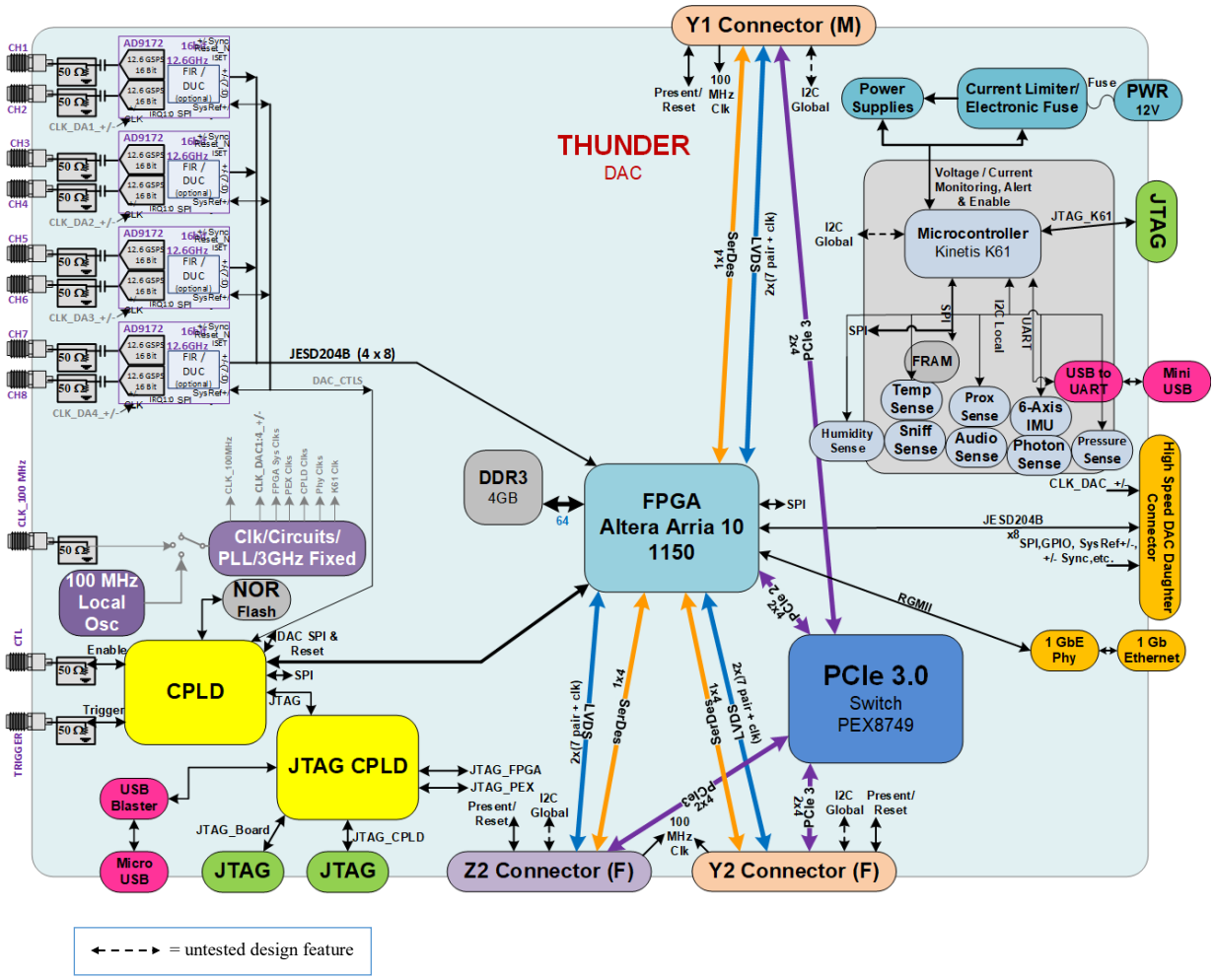
Product Specifications

FPGA	Arria 10 (10AX115U2F45I2SG): IC FPGA 480 I/O 1932FCBGA
	1.366 TFLOPS
	ALMs: 427,200
	LEs (K): 1150
	Registers: 1,708,800
	M20K memory blocks: 54,260
	2x4 Gen2 PCIe interfacing with PEX8479
DAC	8 Channels (2 per DAC chip)
	16 bit, 11.5 GSPS per Channel
	1×, 2×, 3×, 4×, 6×, and 8× Configurable Data Channel Interpolation
	Internal PLL
	Drives 50 Ohm Load
	1.5 GSPS Complex Data per Channel
	48-bit NCO per Channel
Memory—DDR	4GB Unbuffered DDR3
	DDR3 SODIMM, 1600 MT/s
Clocking Options	Onboard Oscillator
	Offboard SMA
Health Monitoring	Board Voltages
	Temperature Monitoring of PCIe Switch, FPGA
	Two External Temperature Sensors
	Monitoring via I2C bus
	Smoke, Humidity, Light/Proximity, Pressure, Audio (untested design feature), 6 -Axis IMU Sensors
Power	Supply Options: 12V Power Cable
	Nominal Power: 40W, MAX: 54W
	Additional Power Features: E-fuse/Continuous Power Monitoring
	I/O Power Levels: - LVDS 1.8V - SERDES & PCIe: High Speed Diff. @ 1.0V - DAC: <5dBm (Typical Testing @ 0 dBm) - Clock Input: 100MHz @ 10 dBm Typical (13 dBm Max)
External Interfaces	2x4 Gen3 PCIE at All Connectors
	Connector Y1, Y2, Z2 all Have Gen3 PCIE, SERDES, and LVDS
	UART, JTAG, GbE (RJ45)
	I2C, Present/Reset Bit Sensing for Slave Mode Operation on all YZ Connectors
Environmental	Operating temperature: 0° to 50°C (Commercial Configuration)
	Storage Temperature : (est) -40°C to 85°C, Cooling AirFlow Recommended, FPGA Application Dependent (Heat Sink Mounts Available)
Physical	Physical Dimensions: 6.25”L x 6.25”W
	Distance Between Boards (Stacked; Board-to-Board): 1.1”

DAC Performance Specs

SFDR	at Fout = 850MHz, SFDR = -85dBc
	at Fout = 943MHz, SFDR = -88dBc
Noise Spectral Density (NSD)	at Fout = 850MHz, NSD = -66dBc/MHz
	at Fout = 942MHz, NSD = -60dBc/MHz
	Balun on Output with 10-8000MHz Freq. Response Range
	Up to ~10GBps JESD204Bx8 Interface with FPGA
	Output Power <5dBm, (Typically Testsed @ 0dBm)

BLOCK DIAGRAM



CONFIGURATIONS

Model Number	Configuration
3DR-A10-DAC-11.5 GSPS -C	Commercial Temp 0°C—50°C

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