



Model Number: 3DR-V6-DAC-1GSPS



3DR COMPUTING OVERVIEW

3DR computing technology brings together high performance computing, ease of programmability, low-cost, and commercial I/O flexibility in a modular, open systems and standards architecture to realize uniquely scalable and widely configurable, high speed embedded processing solutions for the development of radar, EW, SIGINT, and communication systems.

3DR computing possesses the unique ability to morph in size, shape, and processing capacity. This flexibility provides a low cost, standard solution capable of rapidly conforming to the vastly different power, space, and environmental requirements found aboard any surface, sub-surface, or airborne system or platform.

PRODUCT DESCRIPTION

The 3DR-V6-DAC-1GSPS, known as Thunder I, is a 2 channel, 16-bit, 250MHz digital-to-analog converter board used to convert digital signals into analog waveforms. Each channel drives two SMAs. The onboard Virtex-6 FPGA (XC6VLX240T) can be used to digitally generate waveforms or playback pre-stored samples. As with all 3DR computing modules, Thunder I supports three-dimensional connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements. Thunder I also offers additional external interface via Twinax, SMA, and ribbon cable connections for tailored clocking and control signal flexibility. The 3DR computing standard microcontroller architecture is interfaced through the I2C bus to provide FPGA temperature, voltage, and current monitoring for automatic shut-down during critical over heat and/or voltage conditions.

FEATURES APPLICATIONS BENEFITS

FPGA

- Xilinx Virtex 6 (XC6VLX240T)
- Flash memory for up to two FPGA configurations
- LX365T & LX550T available in 1759 package
- JTAG programmable
- 2 NOR flash configuration/user programmable memories (master BPI configuration, write protect available)

Digital -to-Analog Conversion

- 2 channel
- 16-bit
- 250 MHz

I/O Support available via

- X-connector (2x)
- Z-connector (2x)
- Z-SERDES (2x)
- Digital connectors for FPGA direct connection (4x, 100pin)
- JTAG

Tailored Clocking and Control Signal Flexibility

- Clock input (SMA/Twinax)
- 6x programmable SMA (output)
- 4x programmable SMA (bi directional)

Standard 3D Computing

Microcontroller Interface

- Dual microcontrollers programmable over SPI bus
- Controls power-on and power-down sequencing
- Monitors voltages and reports faults over I2C bus
- Monitors current, e-fuse shut-down, and reports over I2C bus
- Monitors board temperature over I2C bus (external sensor available)
- On board EEPROM for data storage and logging (write protect available)
- FPGAs and CPLDs programmable over JTAG Bus (for applicable modules with FPGAs and CPLDs), or via connectors from other 3DR computing boards (firmware required)

- General Purpose/ Digital Signal Processing
- Radar Exciters and Digital Waveform Generation (DWG)
- Electronic Warfare/Attack Systems
- SIGINT (ELINT, COMINT, Etc.) Systems
- Enough FPGA flash memory to hold two FPGA configurations
- On board current limiting circuitry fuse and temperature monitoring for board protection
- Standard 4-pin power connector

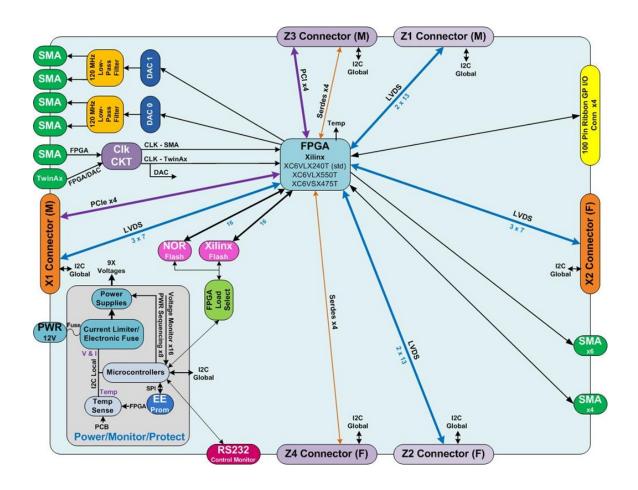


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CONFIGURATIONS

Model Number	Configuration
3DR-V6-DAC-1GSPS-C	Commercial temp 0°C-50°C

^{*}Please contact CEI for extended temperature range options

SPECIFICATIONS

DAC	External Interfaces	Clocking Options
Texas Instruments DAC 5681Z	X1, Z1 connectors: PCIe & LVDS (FPGA)	Onboard oscillator
		Off board SMA
2 channels (1 per device)	X2, Z2 connectors: LVDS (FPGA)	Off board Twinax
16 bit, 250 MHz, 1.0 GSPS	Z3,Z4 connectors: SERDES (FPGA)	Board-to-board Z connector
On-chip 2x/4x interpolation filters	100 pin ribbon cable general purpose (GP)	Environmental
Internal PLL	I/O connectors (80 single ended or 40 differential signals each) : x4	Operating temperature: 0° to 50°C (commercial configuration)
(2x) dual outputs	General purpose SMA outputs from FPGA: x6	Storage temperature: (est) -55°C to 100° cooling airflow recommended, FPGA a
120 MHz cutoff Low Pass Filter	General purpose SMA I/O to/from FPGA: x4	cation dependent (heat sink mounts avai
		Physical
Drives 50 ohm load	Power	Dimensions: 6.25"L x 6.25"W
	Power consumption (based on FPGA loading) 12V @ 2.08 amps	Distance between boards
+/- 1.1 peak-to-peak		(stacked; board-to-board): 1.1"