3DR COMPUTING

Lightning III

8 Channel, 16-bit, 250 MSPS Analog-to-Digital Converter

Model Number: 3DR-A10-ADC-250MSPS

COLORADO ENGINEERING, Inc.

3D COMPUTING OVERVIEW

3DR Computing technology brings together high performance computing, ease of programmability, low-cost, and commercial I/O flexibility in a modular, open systems and standards architecture to realize uniquely scalable and widely configurable, high speed embedded processing solutions for the development of radar, EW, SIGINT, and communication systems.

3DR Computing possesses the unique ability to morph in size, shape, and processing capacity. This flexibility provides a low cost, standard solution capable of rapidly conforming to the vastly different power, space, and environmental requirements found aboard any surface, sub-surface, or airborne system or platform.

PRODUCT DESCRIPTION

The 3DR-A10-ADC-250MSPS, known as Lightning III, is an 8 channel, 16-bit, 250 MSPS Analog to Digital converter board for digitizing and processing analog inputs. High performance, low latency processing can be implemented via the on-board Altera Arria 10 FPGA (10AX115U2F45I2SG).

As with all 3DR Computing modules, Lightning III supports 3 dimensional connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements. Lightning III provides PCIe and LVDS interfaces via the Y and Z connectors to other modules in the 3DR Computing family. It also offers additional external interfaces including SMA connections for clocking and triggering flexibility.

FEATURES

FPGA

- Altera Arria 10 : 10AX115U2F45I2SG
- 4GB DDR

ADC - ADS42JB69

- Dual-Channel 16-bit ADC
- 250 Mega-Samples Per Second (MSPS)
- Data rates up to 3.125 Gbps
- JESD204B Serial Interface with up to Four Lane Support
- SNR: 73.3 dBFS, SFDR 93dBC @ 170MHz, 2Vpp, -1dBFS

External I/O Support available via

- Y-Connector (2x)
- Z-Connector (1x)
- JTAG
- 4x—40 GbE Daughter Card
- SMA
- UART

Tailored Clocking and Triggering Flexibility

- Sample Gates (SMA) In/Out
- Trigger (SMA) In/Out
- Clock Inputs (SMA)
- On-board Clock

Standard 3D Computing

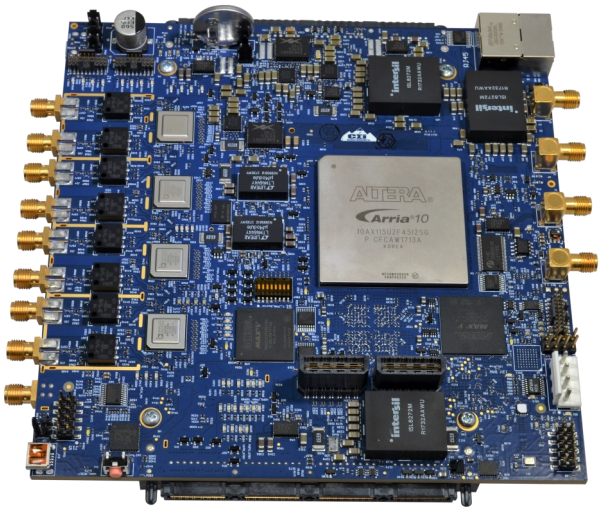
- K61 Microcontroller Interface
- Controls power-on and power-down Sequencing
- Monitors voltages and reports faults over I2C bus
- Monitors current, e-fuse shut-down, and reports over I2C bus
- Monitors board temperature over I2C bus (external sensor available)
- On board EEPROM for Data Storage and logging (write protect available)
- FPGAs and CPLDs programmable over JTAG Bus (for applicable modules with FPGAs and CPLDs), or via connectors from other 3DR Computing boards (Firmware required)

APPLICATIONS

- Digital Signal Processing/ Data Acquisition
- Radar Receiver (Digital Receiver)
- Digital Array Processing & Beamforming
- Electronic Warfare/Attack Systems

BENEFITS

- Enough FPGA Flash Memory to hold two FPGA configurations
- On board circuitry fuse and temperature monitoring for board protection
- Standard 4-pin power connector



intel FPGA Design Solutions Network Platinum

Product Datasheet Revision 111103-1. www.coloradoengineering.com

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SPECIFICATIONS

ADC
Dual Channel, 16– bit
250MSPS

Environmental
Operating temperature : 0° to 50°C (Commercial Configuration)
Storage Temperature : (est) -55°C to 100°C, Cooling AirFlow Recommended, FPGA Application Dependent (Heat Sink Mounts Available)

Memory — DDR
4 GB Unbuffered

Health Monitoring
Board Voltages
PCIe Switch, FPGA
Two External Temperature Sensors
I2C
Smoke/Impact Detection

Power
Power Consumption: 12V @ 15.5 Amps (Subject to FPGA Loading)
Supply Options: 12V Power Cable
Additional Power Features: e-fuse/continuous power monitoring

Clocking Options
Onboard Oscillator
Offboard SMA

Physical
Dimensions: 6.25”L x 6.25”W
Distance Between Boards (Stacked; Board-to-Board) : 1.1”

External Interfaces **
Y1, Y2, Z2 Connectors : PCIe, LVDS (FPGA), and serdes.

CONFIGURATIONS

Model Number	Configuration
3DR-A10-ADC-250MSPS –4-C	8 Channel @ 250 MSPS Each, Commercial Temp 0°C—50°C

	Half Duplex (FPGA LVDS@1.6GHz)			Full Duplex			Bandwidth		
3DR Connector	# of Clusters	# of LVDS Pairs	LVDS Total (MB/s)	PCIe x4 (MB/s)	PCIe x4 (MB/s)	SerDes x4 (MB/s)	Bandwidth per Connector	Total Bandwidth per X, Y, Z	Total Bandwidth per Module
Y1	2	7**	2,800	8,000	8,000	8,000	26.2 GB/s	52.3 GB/s	
Y 2	2	7**	2,800	8,000	8,000	8,000	26.2 GB/s	52.3 GB/s	
Z2	2	7**	1,400	8,000	8,000	8,000	24.8 GB/s	24.8 GB/s	133 GB/s

**C1, C2