3DR COMPUTING

Lightning I

4 Channel, 12-bit, 10GSPS Analog-to-Digital Converter

Model Number: 3DR-A10-ADC-10GSPS

COLORADO ENGINEERING, Inc.

3D COMPUTING OVERVIEW

3DR computing technology brings together high performance computing, ease of programmability, low-cost, and commercial I/O flexibility in a modular, open systems and standards architecture to realize uniquely scalable and widely configurable, high speed embedded processing solutions for the development of radar, EW, SIGINT, and communication systems.

3DR computing possesses the unique ability to morph in size, shape, and processing capacity. This flexibility provides a low cost, standard solution capable of rapidly conforming to the vastly different power, space, and environmental requirements found aboard any surface, sub-surface, or airborne system or platform.

PRODUCT DESCRIPTION

The 3DR-A10-ADC-10GSPS, known as Lightning 1, is a 4 channel, 12-bit, 10GSPS Analog-to-Digital converter board for digitizing and processing analog inputs. High performance, low latency processing can be implemented via the onboard Altera Arria 10 FPGA (10AX115U3F45I2SG).

As with all 3DR computing modules, Lightning 1 supports three dimensional connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements. Lightning 1 provides PCIe and LVDS interfaces via the Y and Z connectors to other modules in the 3DR computing family. It also offers additional external interfaces including Twinax, and SMA connections for clocking and triggering flexibility along with Time of Day (ToD).

FEATURES

FPGA

- Altera Arria 10
- 10AX115U3F45I2SG
- 2x—Hybrid Memory Cube (HMC)

Analog-to-Digital Conversion

- 4x2.5 GSPS channels non-interleaved
- 2x5 GSPS channels interleaved
- 1x10 GSPS channel interleaved
- 12-bit
- >8 ENOB
- Non-linear equalizer IP
- >4 GHz instantaneous bandwidth

Clocking and Triggering Flexibility

- Sample gates (SMA)
- Trigger (SMA)
- Clock inputs (SMA/Twinax)
- ToD—Time of Day

I/O Support available via

- Y-connector (2x)
- Z-connector (1x)
- High speed connector (1x Top)
- JTAG
- 4x—40 GbE daughter card

APPLICATIONS

- Digital signal processing/ data acquisition
- Radar receiver (digital receiver)
- Digital array processing & Beamforming
- Electronic warfare/attack systems

BENEFITS

- Enough FPGA flash memory to hold two FPGA configurations
- On board circuitry fuse and temperature monitoring for board protection
- Standard 4-pin power connector

4 Channel, 2.5 GSPS Non-Interleaved ADC, >8 ENOB
2 Channel, 5 GSPS Interleaved ADC, >8 ENOB *
1 Channel, 10 GSPS Interleaved ADC, >8 ENOB *
*** Requires interleaving board**

intel FPGA Design Solutions Network Platinum

Product Datasheet Revision 111103-1. www.coloradoengineering.com

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SPECIFICATIONS

Memory—HMC	Health Monitoring	Power
• 4/8 GB RAM • 70% less power than DDR3 • Up to 17X Faster than DDR3	• Board voltages • Temperature of K61, PCIe switch, FPGA • Two external temperature sensors • I2C	• Power consumption: 12V @ 15.5 amps (subject to FPGA loading) • Supply options: 12V power cable • Additional power features: e-fuse/ continuous power monitoring

CONFIGURATIONS

Model Number	Configuration
3DR-A10-ADC-10GSPS –4-C	4 Channel @ 2.5 GSPS each, commercial temp 0°C—50°C
3DR-A10-ADC-10GSPS –2-C	2 Channel @ 5 GSPS each, commercial temp 0°C—50°C **
3DR-A10-ADC-10GSPS –1-C	1 Channel @ 10 GSPS, commercial temp 0°C—50°C **

** Check for availability — these configurations require interleaving board
*Please contact CEI for extended temperature range options

	Half Duplex (FPGA LVDS@1.6GHz)			Full Duplex			Bandwidth		
3DR Connector	# of Clus-ters	# of LVDS Pairs	LVDS Total (MB/s)	PCIe x4 (MB/s)	PCIe x4 (MB/s)	SerDes x4 (MB/s)	Bandwidth per Connector	Total Bandwidth per X, Y, Z	Total Bandwidth per Module
Y	2	7	2,800	8,000	8,000	8,000	26.2 GB/s	52.3 GB/s	
Z2	1	7	1,400	8,000	8,000	8,000	24.8 GB/s	24.8 GB/s	133 GB/s
HS	1	6	1,200	8,000	8,000	48,000	55.9 GB/s	55.9 GB/s