3DR COMPUTING

Hurricane

Altera Arria 10, Tegra K1 APU

Model Number: 3DR-A10-GPGPU

COLORADO ENGINEERING, Inc.

PRODUCT DESCRIPTION

The 3DR-A10-GPGPU module, known as Hurricane, follows the 3DR topology, so it can be used in combination with other 3DR-compatible boards to add parallel processing power to a system. The Tegra K1 APU can deliver nearly 300 GFLOPS single precision peak per TK-1 SOM . The Arria 10 can deliver an additional 1333 GFLOPS. A 2-link, 2GB Hybrid Memory Cube connects to the FPGA providing an aggregate memory bandwidth of 60 GB/s. Offboard connectivity includes PCIe Gen3, LVDS, and SERDES in all three dimensions as well as one GbE port (APU) and one 10/100 Ethernet (K61), JTAG, and USB-to-UART. The variety of available standard interfaces promotes network connectivity with a wide range of third party systems and subsystems. This includes commercially available switches and routers and promotes the integration of a system-of-systems in a net-centric environment.

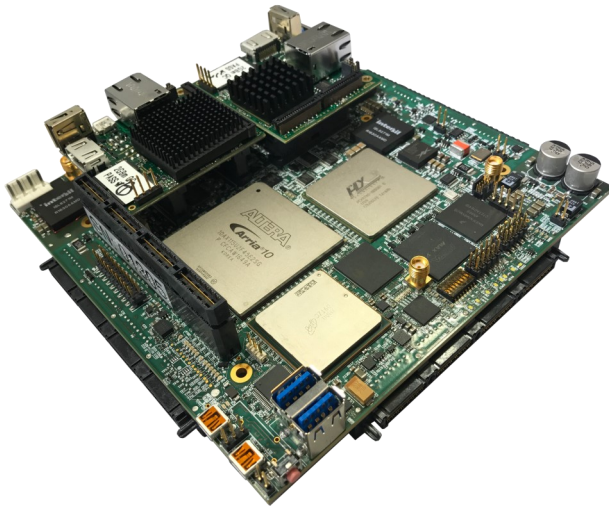
The 3DR standard microcontroller architecture is interfaced through the I2C bus to provide FPGA, APU, GPU, and PCIe switch temperature as well as voltage and current monitoring for automatic shut-down during critical overheat and/or voltage conditions. As with all modules which follow the 3DR topology, the GPU module supports 3-D connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements.

FEATURES

- FPGA: Altera Arria 10, 10AX115U3F45I2SG with 2-Link, 2GB Hybrid Memory Cube. Arria 10 capable of 1333 GFLOPS
- Provides 3D connectivity via PCIe, LVDS, and SerDes with 214.2 GB/sec of bandwidth available per module
- Employs onboard current limiting circuitry and fused temperature monitoring chip
- Additional I/O support available via Gigabit Ethernet, JTAG, and USB-to-UART.
- Gigabit Ethernet (GbE) port support TCP/IP + 2 HDMI + TCIs

APPLICATIONS

- Unmanned Aerial Systems/ Unmanned Ground Systems (UAS/UGS)
- Sensor and navigation processing
- General purpose/digital signal processing
- Radar receiver/exciter
- Digital array processing & beamforming
- Electronic warfare/attack systems
- SIGINT (ELINT, COMINT, etc.) systems
- Digital image processing



intel FPGA Design Solutions Network Platinum

	Half Duplex (FPGA LVDS@1.6GHz)			Full Duplex				Bandwidth		
3DR Connector	# of Clusters	# of LVDS Pairs	LVDS Total (MB/s)	PCIe x4 (MB/s)	PCIe x4 (MB/s)	SerDes x4 (MB/s)	SerDes x1 (MB/s)	Bandwidth per Connector	Total Bandwidth per X, Y, Z	Total Bandwidth per Module
X	2	7	2,800	8,000	8,000	14,200	3,550	35.69 GB/s	71.39 GB/s	
Y	2	7	2,800	8,000	8,000	14,200	3,550	35.69 GB/s	71.39 GB/s	214.16 GB/s
Z	2	7	2,800	8,000	8,000	14,200	3,550	35.69 GB/s	71.39 GB/s	

Product Datasheet Revision 111103-1. www.coloradoengineering.com

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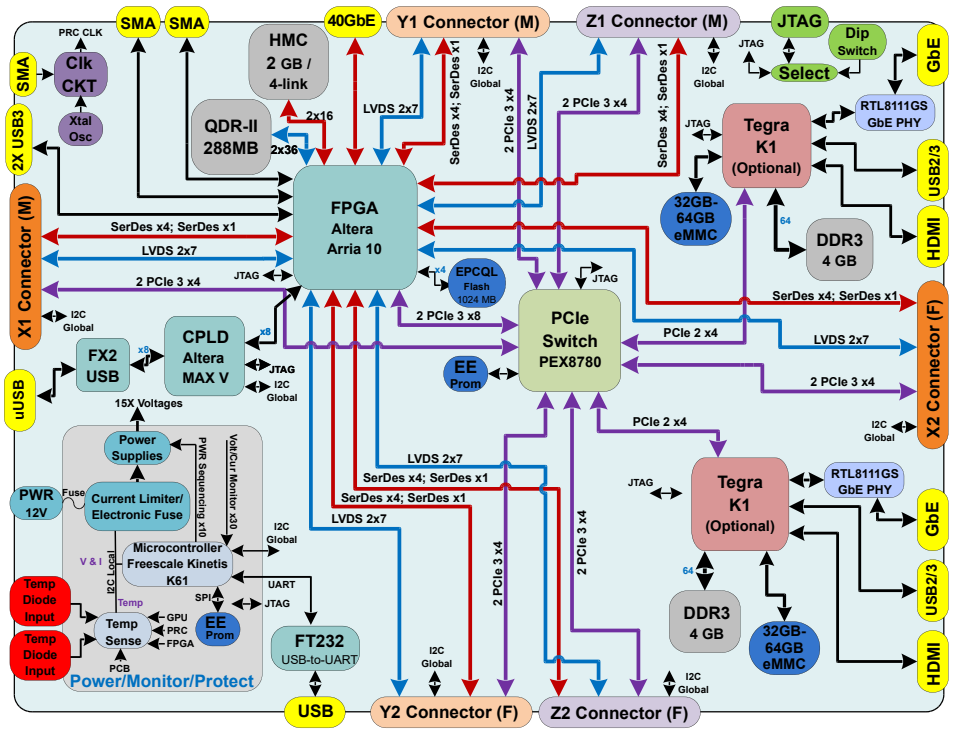
BLOCK DIAGRAM



CONFIGURATIONS

Model Number	Configuration
3DR-A10-GPGPU-C	Commercial temp: 0° - 50° C
3DR GPGPU-C	No Arria 10: 0° - 50° C

*Please contact CEI for extended temperature range options

SPECIFICATIONS

Microcontroller Interface

Controls power-on and power-down sequencing

Monitors voltages and reports faults over 12C bus

Monitors current, e-fuse shut-down, and reports over I2C bus

Monitors board, GPU, FPGA, and PCIe switch temperature over I2C bus (external sensor available)

Onboard EEPROM for data storage and logging (write protect available)

FPGAs and CPLDs programmable over JTAG Bus (for applicable modules with FPGAs and CPLDs

General Characteristics

DDR3: 2, 4, or 8 GB at 1600 MHz

Boot flash: 128MB

FPGA: Altera Arria 10 10AX115U3F45E2SG

JTAG programmable

2-link HMC: 2GB at 60 GB/s

1 GB EPCQL for different configurations

External Interfaces

1G Ethernet ports: 2+

PCI-e (Gen2 or Gen3)

X1, X2 connectors: PCIe (Switch); LVDS (FPGA); Serdes (FPGA)

Y1, Y2 connectors: PCIe (Switch); LVDS (FPGA); Serdes (FPGA)

Z1, Z2 connectors: PCIe (Switch); LVDS (FPGA); Serdes (FPGA)

USB-to-UART

USB-A 2.0 x 2+

USB –A 3.0 x 2+

2x HDMI Ports +

SMA (2in, 1out)

Power

Power Consumption: 12V @ 15 amps (subject to FPGA loading)

Supply Options: 12V Power Cable

Additional power features: e-fuse/continuous power monitoring

Physical

Dimensions: 6.25”L x 6.25”W

Dimensions including connectors: 6.668”L x 6.668” W

Distance Between Boards (Stacked; Board-to-Board) : 1.1”

Environmental

Operating temperature: 0° to +50°C

Storage temperature: (est) -40° to +85°C

Cooling: air flow required; FPGA application dependent

Relative humidity: 10 to 90% non-condensing

Shock/vibration: please contact CEI for configuration options

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