DIGITAL RECEIVER EXCITER

DREX+

COLORADO ENGINEERING, Inc.

High-Performance Digital Receiver/Exciter Plus = Significant DSP Processing

www.ColoradoEngineering.com/DrexPlus

PRODUCT DESCRIPTION

CEI's Digital Receiver/Exciter Plus (DREX+) is designed to meet the demands of next generation Department of Defense (DoD) radar, Electronic Warfare (EW), Signal Intelligence (SIGINT) and communication systems with strict Cost, Size, Weight and Performance (C-SWaP) requirements.

The DREX+ provides eight receive channels with direct digital RF conversion/sampling capability up to 5 GHz in the first Nyquist zone and low 9 GHz at higher Nyquist zones. A selectable super-heterodyne circuit on the RF front end module allows applications through 14 GHz band in the first Nyquist Zone; this also allows for lower sampling ADCs and higher dynamic range. CEI currently has .25, 3 and 10 GSPS ADCs modules. The eight channel exciter is capable of generating direct RF through 6 GHz and with the selectable super-heterodyne up conversion can generate waveforms up to 14 GHz band. This leverages a 12.6 GHz DAC module. The RF DAC channels can feed the ADC inputs for testing, test targets, calibration, dithering, etc. The "+" indicates that the DREX has capabilities beyond the receiver and exciter: three bleeding edge Field Programmable Gate Arrays (FPGAs) and an advanced 24 core General Purpose Processor (GPP) with math acceleration provide unprecedented compute capability, including Digital Signal Processing (DSP) and display system capability.

FEATURES

RF Tx/Rx Signal Conditioning Module

- Input Frequencies from DC to 14GHz
- Direct RF, Nyquist Zone 1, from DC to 6GHz
- Direct RF, Under Sampling, from 1.5GHz to 9GHz
- Super-heterodyne Down Conversion from DC to 14GHz

Analog-to-Digital (ADC) Module

- 8-Channel Input
- Intel (Altera) Arria 10 FPGA with OpenCL BSP
- Multiple ADC options available, including: 250MSPS, 3GSPS and 10GSPS

Digital-to-Analog (DAC) Module

- AD9172
- 8-Channel, 16-bit
- Intel Arria 10 FPGA 10AX115U2F45I2SG

Processor Module

- CEI's 3DR, Modular, High-performance Crestone Processor Module
- NXP (Freescale) T4240 PowerPC (PPC) with 24 Virtual High-performance Cores, Scaling to 1.8GHz and AltiVec Floating Point Vector Math Accelerators
- Intel (Altera) Stratix V FPGA, Optimized for Variable-precision Digital Signal Processing (DSP) and Dynamically Reconfigurable Transceivers
- PCIe Gen 3, LVDS, SerDes and 4X 10GbE Interfaces
- NXP K61 Microcontroller Provides Total System Health Monitoring and Protection

Enclosure

- 3-6U 19" Rack Mountable Server or similar
- MIL-STD Ruggedization
- Approximately 30 lbs.
- Front Panel LED T.V. Screen for Status Control

DREX+ Sample Enclosure

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Performance Specifications

UHF Receiver	**Gain**	49 dB
	Noise Figure	<1.5 dB
	Flatness from 850MHz – 942MHz	±0.725 dB peak-to-peak
	Upper -3dB cutoff frequency	953 MHz
	Isolation between 2 input ports	80 dB
	Max Input Power	No damage for an input signal of +20 dBm
	Max Output Signal	Max output power = 15.76 dBm regardless of input power
	Input VSWR	<1.5:1 across entire band
	OP1dB	13.58 dBm
	IIP3	-16.5 dBm
	OIP3	32.6 dBm
	Temperature Range	0 C to 50 C
	Control / Status Reporting	Via UART
	Power Requirement	6 VDC at 1.51 A
UHF Transmitter	**Frequency Band**	850 to 942 MHz
	Max Output Power	17 dBm
	Group Delay	3 nS.
	Harmonic Rejection	1.5 GHz and 4 GHz, Rejection <60 dBc
	Adjustable Gain / Attenuation	14 db to -15 db 0.5 db steps
	Stop Band Rejection	40 dB above 1300 MHz
	Output VSWR	<1.5:1 across entire band
	Output 1dB Compression	15.5 dBm
	Output IP3	22.94 dBm @ 850 MHz
	Noise Figure	10 dB @ 850 MHz
	Power Requirement	6 VDC at 1.5A
100 MHz to 9 GHz Direct RF RECEIVER	**Gain**	10 dB to 45 dB
	Adjustable Attenuation	60 dB in 1 dB steps
	Noise Figure	<3.5 db across entire band without limiter - add 2.5 dB with limiter
	Flatness from 100MHz—18GHz	±2.5 dB peak-to-peak +/-0.25 dB across any 500 MHz BW
	Isolation between 2 input ports	65 dB
	Max Input Power	+10 dBm
	Max Output Power	10 dBm or less for ADC over drive protection
	Input VSWR	<2:1 across entire band
	OP1dB at ADC input pin	7 dBm
	OIP3 at ADC input pin	17 dBm
	Temperature Range	0 C to 50 C
	Power Requirement	6 VDC at 1A
100MHz to 18GHz Direct RF TRANSMITTER	**Gain**	0 dB to 15 dB or more
	Adjustable Attenuation	15 dB in 0.25 dB steps or 31.5dB in 0.5 dB steps
	Flatness from 100MHz – 18GHz	±2.5 dB peak-to-peak across band +/-0.25 across any 500 MHz BW
	Stop Band Rejection	-40 dB at 32 GHz
	Isolation between two output ports	65 dB
	Max Input Power	+10 dBm

100MHz to 18GHz Direct RF TRANSMITTER Continued	**Max Output Power**	17 dBm
	Output VSWR	<1.5:1 Across Entire Band
	OP1dB	15 dBm
	OIP3	25 dBm
	Digital to Analog Converter Speed	11.5 GHz
	Temperature Range	0 C to 50 C
	Power Requirement	6 VDC at 1A
Selective 500MHz to 18GHz (1100MHZ IF Bandwidth) Superheterodyne RF RECEIVER	**Gain**	10 dB to 45 dB
	Frequency Bandwidth	100 MHz to 20 GHz
	Image rejection DC to 20GHz	>70 dB No image rejection filter required
	Adjustable Attenuation	60 dB in 0.5 dB steps
	Noise Figure	< 3.5 dB across entire band without limiter - add 2.5 dB with limiter
	Final IF Flatness from DC to 1200MHZ	±0.75 dB peak-to-peak.
	Phase Noise	-125 dBc at 10 Khz offset
	Isolation between 2 input ports	65 dB
	Max Input Power	+10 dBm
	Max Output Power	10 dBm or less for ADC Overdrive protection
	Input VSWR	<1.5:1 across entire band
	OP1dB at ADC input pin	7 dBm
	OIP3 at ADC input pin	17dBm
	Temperature Range	0C to 50C
	Power Requirement	6 VDC at 3.5 A
3GHz to 18GHz Superhetero-Dyne RF TRANSMITTER	**Gain**	0 dB to 15 dB
	IF Frequency Response	DC to 5 GHz
	Adjustable Attenuation	15dB in 0.25 dB steps
	RF Gain Flatness from 100MHz – 20GHz	±2.5 dB peak-to-peak across band, +/-0.25 across any 500 MHz BW
	Phase Noise	-125 dBc at 10 KHz offset
	Stop Band Rejection	-40 dB at 35 GHz
	Isolation between two output ports	65 dB
	Max Input Power	+10 dBm
	Max Output Power at 20GHz	+12 dbm
	Output VSWR	<1.5:1 across entire band
	OP1dB at 20GHz	10 dBm
	OIP3 at 20GHz	21 dBm
	Temperature Range	0 C to 50 C
	Power Requirement	6 VDC at 3.5 A

General Block Diagram