3DR COMPUTING

Crestone

Altera Stratix V FPGA Freescale T4240 Processor

Model Number: 3DR-S5-T4240

COLORADO ENGINEERING, Inc.

3DR COMPUTING OVERVIEW

3DR computing technology brings together high performance computing, ease of programmability, low-cost, and commercial I/O flexibility in a modular, open systems and standards architecture to realize uniquely scalable and widely configurable, high speed embedded processing solutions for the development of radar, EW, SIGINT, and communication systems.

3DR Computing possesses the unique ability to morph in size, shape, and processing capacity. This flexibility provides a low cost, standard solution capable of rapidly conforming to the vastly different power, space, and environmental requirements found aboard any surface, sub-surface, or airborne system or platform.

FEATURES

- Altera Stratix V 5SGS-ED8N1F45I2N
- Free Scale T4240 (1.8 GHz)
- Freescale K61
- PLX PCIe 3D Mesh
- SerDes 3D Mesh
- LVDS 3D Mesh
- DDR3: 12GB DDR3@1600
- MT/s (3 memory controllers with 4GB each)
- NAND flash: 512MB
- PPC local bus: up to 100MHz at 16 bits

APPLICATIONS

- General purpose
- Digital signal processing
- Radar receiver/exciter
- Electronic warfare/attack systems
- Digital array processing & beamforming
- SIGINT (ELINT, COMINT, etc.)
- Systems digital image processing

  remote sensing

intel FPGA Design Solutions Network Platinum

PRODUCT DESCRIPTION

At the heart of the 3DR family architecture is the 3DR-S5-T4240 processor module, known as Crestone. This module consists of a power PC (Freescale T4240) general purpose and communications processor, an Altera Stratix V FPGA, on board DDR3 memory modules, and a combination of PCIe Gen 3, LVDS, and SERDES commercially available I/O modules. The processing modules also provide dual 10G Ethernet ports, JTAG, and UART-over-USB. The variety of available standard interfaces promotes network connectivity with a wide range of third party systems and subsystems. This includes commercially available switches and routers and promotes the integration of a system-of-systems in a net-centric environment.

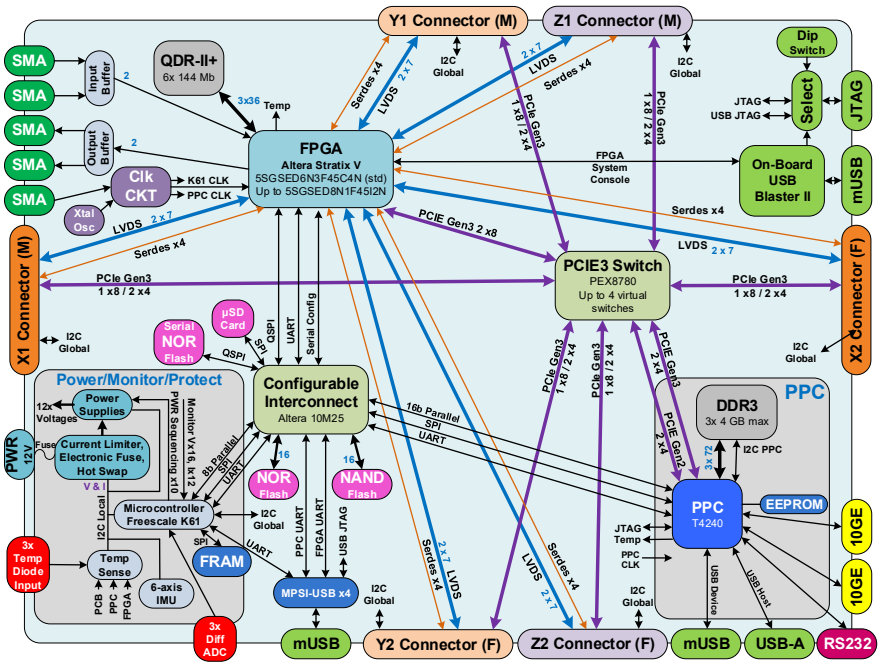
The 3DR standard micro-controller architecture is interfaced through the I2C bus to provide FPGA and PPC temperature, voltage, current, and clock monitoring for automatic shut-down during critical over heat and/or voltage conditions. As with all 3DR modules, Crestone board supports 3D connectivity, allowing the user to stack and/or tile modules to address a wide variety of processing, I/O, size, weight, and power requirements.

	Half Duplex (FPGA LVDS@1.6GHz)				Full Duplex			Bandwidth		
3DR Connector	# of Clusters	# of LVDS Pairs	LVDS Total (GB/s)	LVDS Total (MB/s)	PCIe x4 (MB/s)	PCIe x4 (MB/s)	SerDes x4 (MB/s)	Bandwidth per Connector	Total Bandwidth per X, Y, Z	Total Bandwidth per Module
X	2	7	22,400	2,800	8,000	8,000	8,000	26.8 GB/s	53.6 GB/s	160.8 GB/s
Y	2	7	22,400	2,800	8,000	8,000	8,000	26.8 GB/s	53.6 GB/s	160.8 GB/s
Z	2	7	22,400	2,800	8,000	8,000	8,000	26.8 GB/s	53.6 GB/s	160.8 GB/s

Product Datasheet Revision 111103-1. www.coloradoengineering.com

1915 Jamboree Dr., Colorado Springs, CO 80920 | (719)388-8582 | sales@coloradoengineering.com | www.ColoradoEngineering.com

BLOCK DIAGRAM



CONFIGURATIONS

Model Number	Configuration
3DR-S5-T4240-P	T4240 only, no StratixV
3DR-S5-T4240-C	Commercial Temp — 0°C - 50°C
3DR-S5-T4240-S	Trusted computing platform version
3DR-Cables	6” high speed inter-module cables

*Please contact CEI for extended temperature range options

SPECIFICATIONS

Altera Stratix V FPGA

- 864 Mb QDR-II+
- LVDS
- SerDes
- PCIe Gen3
- JTAG Programmable
- Master BPI Configuration
- Write Protect Available
- QDR-II+: 576Mb at 450 MT/s

FreeScale T4240

- 12 cores/24 virtual cores
- 2 - 10 GbE Ports
- PCIe Gen 2

External Interfaces

- Two 10G Ethernet ports
- Gen 3 PCIe (single x8 or dual x4 per connector)
- All X, Y, Z connectors
- FPGA: SERDES, LVDS, PCIE
- PPC: PCIE
- RS-232: PPC
- UART-over-USB: PPC
- Microcontroller, FPGA

Power

- Power consumption: 12V @ 6Amps (subject to FPGA loading)
- Supply options : 12V power cable
- Additional power features: e-fuse/continuous power monitor-ing

Physical

- Board dimensions: 6.25” L x 6.25” W
- Board dimensions with connectors: 6.668” L x 6.668” W
- Distance between boards (stacked, board-to-board): 0.990”
- Weight: 12.2 oz

Environmental

- Operating temperature:
- 0°C to +50°C
- Storage temperature: (est)
- -40°C to +105°C
- Cooling: airflow recommended, FPGA application dependent
- Relative humidity: 10% to 90% non condensing
- Shock/Vibration: please contact CEI for configuration options

SerDes 3D Mesh

- x4 SerDes
- 56 Gbps per connector
- 56 Gbps in X connectors
- 56 Gbps in Y connectors
- 56 Gbps in Z connectors

LVDS 3D Mesh

- 2 clusters of 7 LVDS per connector
- 14 Gbps in X
- 14 Gbps in Y
- 14 Gbps in Z

FreeScale K61

- Controls power sequencing
- Monitors temperatures
- Monitors voltages
- Monitors currents

PLX PCIe 3D Mesh

- 8,000 MBps full duplex per connector
- 1x8 or 2x4 per connector
- 16,000 MB/s in X Connectors
- 16,000 MB/s in Y Connectors
- 16,000 MB/s in Z Connectors

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